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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,482	03/31/2004	Toshiharu Furukawa	ROC920030399US1	6082

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EXAMINER	
GOODWIN, DAVID J	

ART UNIT	PAPER NUMBER
2818	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/814,482	FURUKAWA ET AL.	
	Examiner	Art Unit	
	David Goodwin	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-11 and 13-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Wasshuber (US2003/0111699).

3. Wasshuber teaches a semiconductor device. Said device comprises an island (524) of semiconductor material having a plurality of sidewalls and a strained region (paragraph 0031-0032) (fig 22). A handle wafer (514) and an insulating layer (512) disposed between said island (524) and said handle wafer (514). Said insulating layer (512) containing a thick region underlying the strained semiconductor island (524) and said insulating layer (512) electrically isolating said island (524) of said semiconductor material from said handle wafer (514). The underlying thickness of insulator exerts a tensile stress on the strained region (524) (paragraph 0042-0043).

4. Regarding claim 2.

5. Said insulating layer (512) comprises a buried oxide layer and said island is silicon (paragraph 0020-0021).

6. Regarding claim 3.

7. Wasshuber teaches a source (522a) and drain (522b) defined in the island (524), and a channel defined in the island between said source and said drain (fig 22) (paragraph 0034-0036). Said channel is disposed at least partially in said strained region of said island (fig 22) (paragraph 0042-0043).

8. Regarding claim 4.

9. Wasshuber teaches that the gate electrode (540) is isolated from said portion of the island (524) defining said channel (fig 22) (paragraph 0042-0043).

10. Regarding claim 5.

11. Wasshuber teaches that the insulating material (12b) divides the gate electrode (32) there being equal portions of the gate on each side of of the midpoint of the straining layer(fig 1) (paragraph 0020-0022).

12. Regarding claim 6.

13. Wasshuber teaches that the gate electrode overlies the channel (fig 22).

14. Regarding claim 7.

15. Wasshuber teaches that that the structure comprises a semiconductor device (fig 22) (paragraph 000042-0043).

16. Regarding claim 8.

17. Wasshuber teaches that the island (524) comprises silicon and the thickened region of underlying insulator (512) comprises silicon dioxide (paragraph 0020-0021).

18. Regarding claim 9.

19. Wasshuber teaches that the underlying insulator comprises silicon dioxide (paragraph 0020-0021).

20. Regarding claim 10.

21. Wasshuber teaches that the wafer (514) comprises silicon and the thickness of underlying insulator (512) comprises silicon dioxide (paragraph 0020-0021).

22. Regarding claim 11.

23. Strained silicon enhances carrier mobility (0003).

24. Regarding claim 13.

25. The thickened region of said insulating layer (512) has a thickness greater than the surrounding insulating layer flanking said region, see the central portion of layer 512 and the ends of said layer (512) (fig 22).

26. Regarding claim 14.

27. First and second anchors, comprising the portions of semiconductor overlying the ends of the thickened layer (512), flanking the strained region prevent relaxation of the strain region (fig 22).

28. Regarding claim 15.

29. First and second anchors flanking, comprising the portions of semiconductor overlying the ends of the thickened layer (512), and adjacent to the strained region prevent relaxation of the strain region (fig 22).

30.

31. Claims 1-4, 6-12, 14 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Yeo (US 2004/0150042).

32. Regarding claim 1

33. Yeo teaches a semiconductor device. Said device comprises an island (84) of semiconductor material having a plurality of sidewalls and a strained region (paragraph 0031-0032) (fig 3D). A handle wafer (52) and an insulating layer (54) disposed between said island (84) and said handle wafer (52). Said insulating layer (54) containing a thick region underlying the strained semiconductor island (84) and said insulating layer electrically isolating said island (84) of said semiconductor material from said handle wafer (52). The underlying thickness of insulator exerts a tensile stress on the strained region (84) (paragraph 0031).

34. Regarding claim 2.

35. Said insulating layer (54) comprises a buried oxide layer and said island is silicon (paragraph 0031).

36. Regarding claim 3.

37. Yeo teaches a source defined in the island, a drain defined in the island, and a channel defined in the island between said source and said drain (fig 5) (paragraph 0034-0036). Said channel is disposed at least partially in said strained region of said island (fig 5).

38. Regarding claim 4.

39. Yeo teaches that the gate electrode is isolated from said portion of the island (84) defining said channel (fig 5) (paragraph 0036).

40. Regarding claim 6.

41. Yeo teaches that the gate electrode overlies the channel (fig 5).

42. Regarding claim 7.

43. Yeo teaches that that the structure comprises a semiconductor device (fig 5) (paragraph 0036).

44. Regarding claim 8.

45. Yeo teaches that the island comprises silicon and the thickness of underlying insulator comprises silicon dioxide (fig 0031).

46. Regarding claim 9.

47. Yeo teaches that the thickness of underlying insulator comprises silicon dioxide (fig 0031).

48. Regarding claim 10.

49. Yeo teaches that the wafer comprises silicon and the thickened region of underlying insulator comprises silicon dioxide (fig 0031).

50. Regarding claim 11.

51. Strained silicon enhances carrier mobility (0002).

52. Regarding claim 12.

53. The thickness of oxide material is more than 5 to 10 nanometers.

54. Regarding claim 14.

55. First and second anchors, comprising the portions of semiconductor overlying the ends of the thickened layer (512), flanking the strained region prevent relaxation of the strain region (fig 5).

56. Regarding claim 15.

57. First and second anchors, comprising the portions of semiconductor overlying the ends of the thickened layer (512), flanking and adjacent to the strained region prevent relaxation of the strain region (fig 5).

Response to Arguments

58. Applicant's arguments filed 3/15/07 have been fully considered but they are not persuasive.

59. The applicant argues Washubar does not teach the formation of a thickened insulating layer. The applicant further notes that Washubar teaches the implantation of oxygen into a buried layer.

60. The applicant will note that when oxygen is implanted into silicon to form a buried layer, said buried layer will comprise silicon oxide by a means known to one of ordinary skill in the art as a chemical reaction. Silicon oxide is an insulator which is known to one of ordinary skill in the art to have insulating properties, which as the applicant notes are different than semiconductors.

61. The applicant argues that Wasshuber does not teach a a thickened layer.

62. The applicant will note that Wasshuber explicitly states that the buried layer comprises a volumetric expansion (paragraph 0035).

63. The applicant will note that when a layer undergoes a volumetric expansion it "thickens."

64. The applicant argues that Wasshuber does not teach that any part of the buried layer undergoes more thickeneing than any other part of said layer.

65. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., a thickening differential) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

66. The applicant argues that Wasshuber does not teach electrically isolating the semiconducting island.

67. The applicant will note, in figure 20, electrically isolating trenches (531a,b) and electrically isolating buried oxide (512). One of ordinary skill in the art would understand that a semiconducting island surrounded by electrically isolating structures is an electrically isolated semiconducting island.

Conclusion

68. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Goodwin whose telephone number is (571)272-8451. The examiner can normally be reached on Monday through Friday, 9:00am through 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on (571)272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DJG

STEVEN LOKE
SUPERVISORY PATENT EXAMINER

Steven Loke